

What is claimed is:

1. A semiconductor device comprising:

a first transistor having a first gate put between a first source and a first drain;

5 a second transistor arranged adjacent to said first transistor, said second transistor having a second gate put between a second source and a second drain, said second gate arranged parallel to said first gate;

a first dummy gate arranged between said first drains and said second source and parallel to said first gate;

10 a second dummy gate arranged adjacent to said first source and parallel to said first gate; and

a third dummy gate arranged adjacent to said second drain and parallel to said first gate.

2. The semiconductor device according to claim 1, wherein said first and second gate, said first, second and third dummy gate are the same as each other in shape.

3. The semiconductor device according to claim 1, wherein said first and second gate, said first, second and third dummy gate are evenly spaced.

4. The semiconductor device according to claim 1, wherein said first and second gate are respectively three-forked.

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5. A semiconductor device comprising:

a first transistor having

a first source,

a first drain,

5 a first gate arranged between said first source and first drain,

a first contact hole formed on said first source and arranged at a first distance from said first gate, and

10 a second contact hole formed on said first drain and arranged at a second distance from said first gate, said second distance being the same with said first distance; a second transistor arranged parallel to said first gate and having

a second source,

15 a second drain,

a second gate arranged between said second source and second drain,

a third contact hole formed on said second source and arranged at a third distance from said second gate, and

20 a fourth contact hole formed on said second drain and arranged at a fourth distance from said second gate, said fourth distance being the same with said third distance;

a first dummy gate set between said first drain and said second source and parallel to said first gate;

25 a second dummy gate set next to said first source and parallel to said first gate; and

a third dummy gate set next to said second drain and parallel to said first gate.

6. A semiconductor device including first and second transistors each having terminal commonly connected to a node; said device comprising:

a first gate electrode layer of said first transistor;

5 a first electrode layer of said first transistor coupled to a first contact hole;

a second electrode layer of said first transistor coupled to a second contact hole;

a second gate electrode layer of said second transistor;

10 a third electrode layer of said second transistor coupled to a third contact hole;

a fourth electrode layer of said second transistor coupled to fourth contact hole, said fourth electrode layer electrically coupled to said second electrode layer as said  
15 terminal;

wherein said first gate electrode layer, said first electrode layer, said second electrode layer, said second gate electrode layer, said third electrode layer, and said fourth electrode layer are arranged so that a first distance  
20 between said first contact hole and said first gate electrode layer keeps the same with a second distance between said third contact hole and said second gate electrode, and a third distance between said second contact hole and said first gate electrode layer keeps the same with a fourth distance between

25 said fourth contact hole and said second gate electrode layer while a mask for forming said first to fourth contact hole is misaligned.

7. The device as claimed in claim 6, wherein said first electrode layer, said first gate electrode layer, said second electrode layer, said third electrode layer, said second gate electrode layer, and said fourth electrode layer are arranged in that order in a line.

8. The device as claimed in claim 7, wherein said first electrode layer is a source of said first transistor, said second electrode layer is a drain of said first transistor, said third electrode layer is a source of said second transistor, and said fourth electrode layer is a drain of said second transistor.

9. The device as claimed in claim 8, said device further comprising:

a first dummy layer arranged between said second and third electrode layers;

5 a second dummy layer arranged so that said first electrode layer is sandwiched between said second dummy layer and said first gate electrode layer; and

a third dummy layer arranged so that said fourth electrode layer is sandwiched between said third dummy layer and said second gate electrode layer.

10. A semiconductor device comprising:

a first source diffusion region;

a first drain diffusion region;

a second source diffusion region;

5 a second drain diffusion region;

said first source diffusion region, said first drain diffusion region, said first source diffusion region, and said second drain diffusion region being arranged in that order on a line extending in a first direction, said first and second source diffusion regions and said first and second drain diffusion regions being surrounded by an element isolation region;

10 a first gate electrode formed between said first source and drain diffusion regions and extending in a second direction perpendicular to said first direction;

15 a second gate electrode formed between said second source and drain diffusion regions and extending in said second direction;

20 a first source electrode formed over said first source diffusion region and connected with said first source diffusion region through a first contact hole;

a first drain electrode formed over said first drain diffusion region and connected with said first drain diffusion region through a second contact hole;

25 a second source electrode formed over said second source diffusion region and connected with said second source diffusion region through a third contact hole;

a second drain electrode formed over said second drain diffusion region and connected with said second drain  
30 diffusion region through a fourth contact hole.

11. The device as claimed in claim 10, said device further comprising:

a first dummy gate electrode arranged between said first drain and said second source electrodes on said element  
5 isolation region;

a second dummy gate electrode arranged on said element isolation region so that said first source electrode is sandwiched between said second dummy layer and said first gate electrode; and

10 a third dummy layer arranged on said element isolation region so that said second drain electrode is sandwiched between said third dummy layer and said second gate electrode.

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12. The device as claimed in claim 11, wherein said first transistor includes said first source diffusion region, said first drain diffusion region, and said first gate electrode as one of N channel transistor pair and said second transistor  
5 includes said second source diffusion region, said second drain diffusion region, and said second gate electrode as the other of said N channel transistor pair electrically to connect said first drain electrode with said second drain electrode.

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